Serial No.: 09/335,618
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APPENDIX - A

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Twice Amended) A packaged semiconductor device comprising:

a semiconductor die[chip];

a laminate defining first and second major faces, said laminate including

an electrically conductive layer,

an underlying substrate supporting said electrically conductive layer, and

at least one void formed in said laminate so as to extend from said first major face through said electrically conductive layer, through said underlying substrate and through said second major face; and

an encapsulant positioned to mechanically couple said semiconductor die to said first major surface of said laminate, wherein said encapsulant is further positioned to extend through said void from said first major face to said second major face and contacting said underlying substrate.

6. (Amended) A packaged semiconductor device as claimed in claim 1 wherein said semiconductor die[chip] is supported by said laminate and wherein said encapsulant and said laminate are arranged to enclose substantially all of said semiconductor chip.

7. (Twice Amended) A packaged semiconductor device comprising:

a semiconductor die[chip];

a laminate defining first and second major faces, said laminate including

a solder resist layer,

an underlying substrate,

an electrically conductive layer interposed between said solder resist layer

and said underlying substrate, and

at least one void formed in said laminate so as to extend from said first major face through said solder resist layer, through said electrically conductive layer, through said underlying substrate and through said second major face; and

an encapsulant positioned to mechanically couple said semiconductor die to said first major face of said laminate, wherein said encapsulant is further positioned to extend into said void so as to contact said underlying substrate.

8. (Amended) A packaged semiconductor device comprising:

a semiconductor die[chip];

a laminate defining first and second major faces and including a plurality of laminated layers, said laminate including at least one void formed therein so as to extend from one of said major faces through a plurality of said laminated layers; and

an encapsulant positioned to mechanically couple said semiconductor die to said first major face of said laminate, wherein said encapsulant is further positioned to extend into said void across said plurality of laminated layers so as to contact a portion of said laminate between said first and second major faces of said laminate.

12. (Amended) A packaged semiconductor device as claimed in claim 8 wherein said semiconductor die[chip] is supported by said laminate and wherein said encapsulant and said laminate are arranged to enclose substantially all of said semiconductor die[chip].

13. (Twice Amended) A packaged semiconductor device comprising:

a semiconductor die[chip];

an [FR-4 epoxy-glass] epoxy resin glass-cloth laminate defining first and second major faces and including a plurality of laminated epoxy layers, said epoxy laminate including at least

one void formed therein so as to extend from one of said major faces through a plurality of said laminated epoxy layers; and

an encapsulant positioned to mechanically couple said semiconductor die to said first major face of said epoxy resin glass-cloth laminate, wherein said encapsulant is further positioned to extend into said void across said plurality of laminated epoxy layers so as to contact a portion of said laminate between said first and second major faces of said laminate.

23. (Twice Amended) A computer including at least one packaged semiconductor device comprising:

a semiconductor die[chip];

a laminate defining first and second major faces, said laminate including

an electrically conductive layer,

an underlying substrate supporting said electrically conductive layer,

at least one void formed in said laminate so as to extend from said first major face through said electrically conductive layer, through said underlying substrate, and through said second major face; and

an encapsulant positioned to mechanically couple said semiconductor die to said first major face of said laminate, wherein said encapsulant is further positioned to extend into said void so as to contact said underlying substrate.